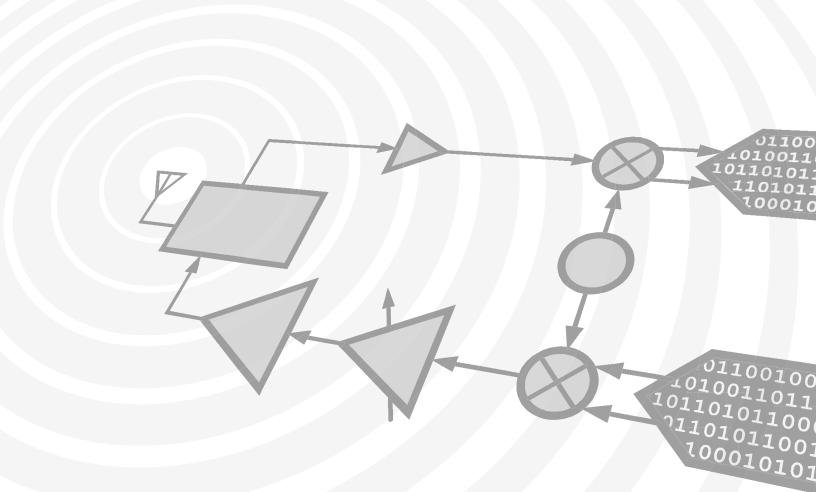




Analog Devices Welcomes Hittite Microwave Corporation

NO CONTENT ON THE ATTACHED DOCUMENT HAS CHANGED







HMC268LM1

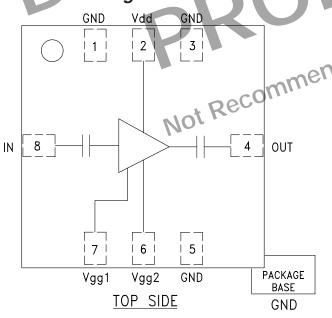
SMT MMIC LOW NOISE AMPLIFIER, 20 - 32 GHz

Typical Applications

The HMC268LM1 LNA enables economical PCB SMT assembly for:

- Millimeterwave Point-to-Point Radios
- LMDS
- SATCOM

Functional Diagram



Features

SMT mmWave Package

Excellent Noise Figure: 2.6 dB

15 dB Gain

P1dB Output Power: +13 dBm

General Description

The HMC268LM1 is a two stage GaAs MMIC Low Noise Amplifier (LNA) in a SMT leadless chip carrier package covering 20 to 32 GHz. The LM1 is a true surface mount broadband millimeterwave package offering low loss & excellent I/O match, preserving MMIC chip performance. Utilizing a GaAs PHEMT process the device offers 2.6 dB noise figure, 15 dB gain and +13 dBm output power from a bias supply of +4V @ 45 mA. As an alternative to chip-and-wire hybrid assemblies the HMC268LM1 eliminates the need for wirebonding, thereby providing a consistent connection interface for the customer. All data is with the non-hermetic, epoxy sealed LM1 packaged LNA device mounted in a 50 ohm test fixture.

Electrical Specifications, $T_A = +25^{\circ} C$, $Vdd = +4V^*$

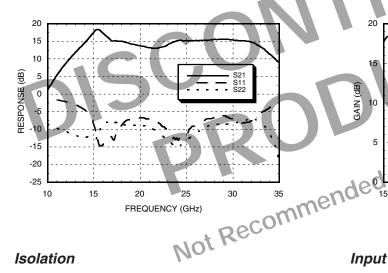
Parameter	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Units
Frequency Range**	20 - 26			26 - 30			30 - 32			GHz
Gain	11	14	17	13	15	18	12	15	18	dB
Noise Figure		2.5	3.2		2.6	3.4		2.8	3.8	dB
Input Return Loss		8			7			7		dB
Output Return Loss		12			8			7		dB
Reverse Isolation	26	33		23	28		23	28		dB
Output Power for 1 dB Compression (P1dB)	7	11		9	13		9	13		dBm
Saturated Output Power (Psat)	13	16		14	17		15	18		dBm
Output Third Order Intercept (IP3)	13	22		17	22		15	21		dBm
Supply Current (Idd)		45	50		45	50		45	50	mA

^{*} Vdd = +4V, adjust Vgg1 & Vgg2 between -2.0 to 0.0 Vdc to achieve ldd = 45 mA.

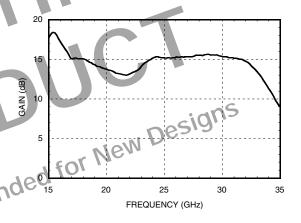
^{**} Acceptable gain and NF performance is achievable down to 17 GHz.



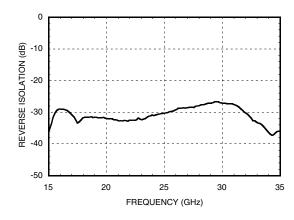
Broadband Gain & Return Loss



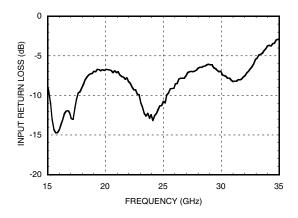
Gain



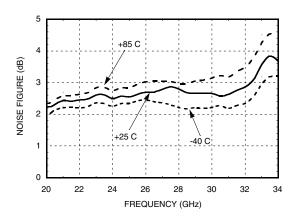
Isolation



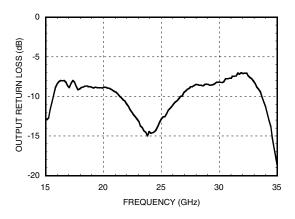
Input Return Loss



Noise Figure

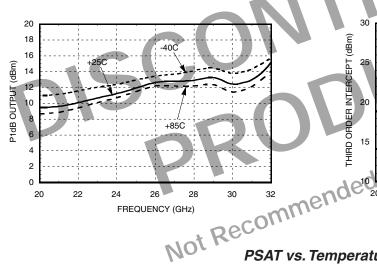


Output Return Loss

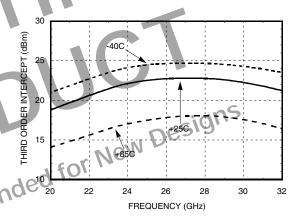




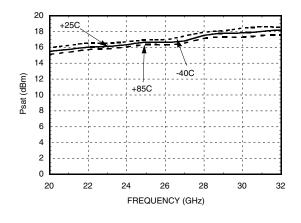
Output P1dB vs. Temperature



Output IP3 vs. Temperature



PSAT vs. Temperature

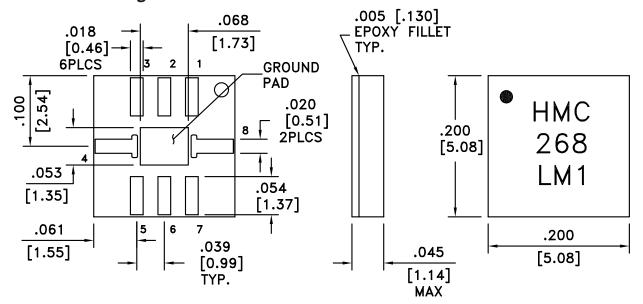




Absolute Maximum Ratings

Supply Voltage (Vdd)	+4.5 Vdc
Supply Current (Idd)	50 mA
Gate Bias Voltage (Vgg1 & 2)	-2.0 to 0.0 Vdc
DC Gate Current (lgg1 & 2)	4 mA
Input Power (RFin) (Vdd = +4V, RF power applied <1 sec)	+15 dBm. 175 °C 289 °C/W -65 to +150° C -40 to +85° C
Channel Temperature (Tc)	175 °C Design
Thermal Resistance (⊖jc) (Channel Backside)	289 °C/W
Storage Temperature	-65 to +150° C
Operating Temperature	-40 to +85° C
N	ot Res

Outline Drawing



Pin	Function		
1	GND		
2	Vdd		
3	GND		
4	RF OUT		
5	GND		
6	Vgg2		
7	Vgg1		
8	RF IN		

- 1. MATERIAL: PLASTIC
- 2. PLATING: GOLD OVER NICKEL.
- 3. DIMENSIONS ARE IN INCHES (MILLIMETERS).
- 4. ALL TOLERANCES ARE ±0.005 (±0.13).
- 5. ALL GROUNDS MUST BE SOLDERED TO THE PCB RF GROUND.
- 6. INDICATES PIN 1



HMC268LM1 Evaluation PCB C2 C2 C2 C3 Not Revolution PCB Not Revolution PCB

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C2

LM1 Evaluation PCB

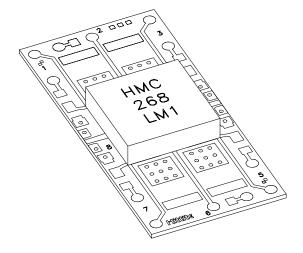
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C2

The grounded Co-Planar Wave Guide (CPWG) PCB input/output transitions allow use of Ground-Signal-Ground (GSG) probes for testing. Suggested probe pitch is 400um (16 mils). Alternatively, the board can be mounted in a metal housing with 2.4 mm coaxial connectors.

Evaluation Circuit Board Layout Design Details

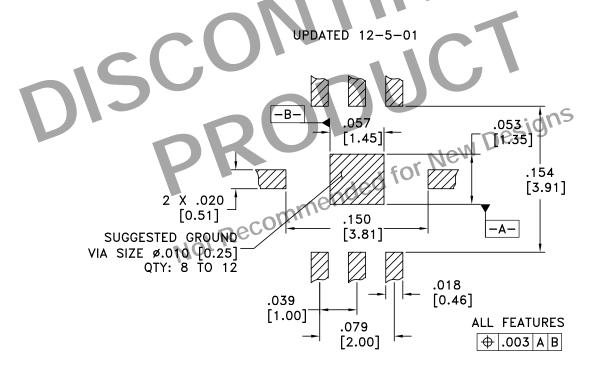
Layout Technique	Micro Strip to CPWG
Material	Rogers 4003 with 1/2 oz, Cu
Dielectric Thickness	0.008" (0.20 mm)
Microstrip Line Width	0.018" (0.46 mm)
CPWG Line Width	0.016" (0.41 mm)
CPWG Line to GND Gap	0.005" (0.13 mm)
Ground Via Hole Diameter	0.008" (0.13 mm)
C1	100 pF Capacitor, 0402 Pkg.
C2	10,000 pF Capacitor, 1206 Pkg.



LM1 Package Mounted to Evaluation PCB



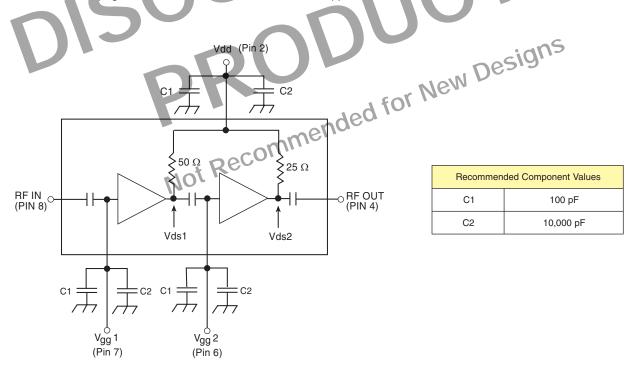
Suggested LM1 PCB Land Pattern Tolerance: ± 0.003" (± 0.08 mm)





HMC268LM1 General Biasing & Application Circuit

Optimal biasing of the HMC268LM1 SMT two stage low noise amplifier Vdd, Vgg1 & Vgg2 DC ports is described below. The LNA schematic is repeated below. Note the recommended addition of the external bypass chip capacitors. For additional general MMIC amplifier biasing guidance, please refer to the Hittite Microwave "MMIC Amplifier Biasing Procedure" found on page 8-8 or on www.hittite.com under the Application Note section.



IMPORTANT DC LIMITS! When biasing the HMC268LM1 please note the following:

- A) Do not exceed 3.5 Vdc on internal circuit nodes Vds1 and Vds2 (internal Drain to Source voltages). Calculate the Vds1 & 2 voltages from the LNA schematic above.
- B) Do not bias Vdd, Vgg1 & Vgg2 DC ports in such a way that Vgs becomes a positive voltage (internal Gate to Source voltage).

HMC268LM1 Biasing Schemes for Performance Trade-Offs

The biasing may be adjusted slightly to achieve either low noise with lowest DC power consumption or low noise with highest output power. Be sure to adhere to the *IMPORTANT DC LIMITS* above while optimizing performance.

- A) Low Noise and Low Power Consumption: Vdd = 3.5 Vdc @ ldd = 30 mA. Set Vgg1 = Vgg2.
- B) Low Noise and High Output Power: Vdd = 4.0 Vdc @ Idd = 45 mA. Utilizing Vgg1 & Vgg2 nominal bias is obtained for a typical Idd current of 30 mA for the second or "output" stage and 15 mA for the first stage. The first step to bias the amplifier is to tune the Vgg1 = -1.0 Vdc and Vgg2 to drive 30 mA for the full amplifier. Then Vgg1 is reduced to obtain Idd = 45 mA of current for the amplifier.



HMC268LM1 Recommended SMT Attachment Technique

Preparation & Handling of the LM1 Millimeterwave Package for Surface Mounting

The HMC LM1 package was designed to be compatible with high volume surface mount PCB assembly processes.

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The LM1 package requires a specific mounting pattern to allow proper mechanical attachment and to optimize electrical performance at millimeterwave frequencies. The PCB layout pattern can be found on each LM1 product data sheet. It can also be provided as an electronic drawing upon request from Hittite Sales & Application Engineering.

Follow these precautions to avoid permanent damage: *Cleanliness:* Observe proper handling procedures to ensure clean devices and PCBs. LM1 devices should remain in their original packaging until component placement to ensure no contamination or damage to RF, DC & ground contact areas.

Static Sensitivity: Follow ESD precautions to protect against ESD strikes.

© 175 H 150 DLY 125 H 100 FO 25 0 1 2 3 4 5 6 7 TIME (min)

Recommended solder reflow profile for HMC LM1 SMT package

General Handling: Handle the LM1 package on the top with

a vacuum collet or along the edges with a sharp pair of bent tweezers. Avoid damaging the RF, DC, & ground contacts on the package bottom. Do not apply excess pressure to the top of the lid.

Solder Materials & Temperature Profile: Follow the information contained in the application note. Hand soldering is not recommended. Conductive epoxy attachment is not recommended.

Solder Paste

Solder paste should be selected based on the user's experience and should be compatible with the metallization systems used. See the LM1 data sheet Outline drawing for pin & ground contact metallization schemes.

Solder Paste Application

Solder paste is generally applied to the PCB using either a stencil printer or dot placement. The volume of solder paste will be dependent on PCB and component layout and should be controlled to ensure consistent mechanical & electrical performance. Excess solder may create unwanted electrical parasitics at high frequencies.

Solder Reflow

The soldering process is usually accomplished in a reflow oven but may also use a vapor phase process. A solder reflow profile is suggested above.

Prior to reflowing product, temperature profiles should be measured using the same mass as the actual assemblies. The thermocouple should be moved to various positions on the board to account for edge and corner effects and varying component masses. The final profile should be determined by mounting the thermocouple to the PCB at the location of the device.

Follow solder paste and oven vendor's recommendations when developing a solder reflow profile. A standard profile will have a steady ramp up from room temperature to the pre-heat temperature to avoid damage due to thermal shock. Allow enough time between reaching pre-heat temperature and reflow for the solvent in the paste to evaporate and the flux to completely activate. Reflow must then occur prior to the flux being completely driven off. The duration of peak reflow temperature should not exceed 15 seconds. Packages have been qualified to withstand a peak temperature of 235°C for 15 seconds. Verify that the profile will not expose the device to temperatures in excess of 235°C.

Cleaning

A water-based flux wash may be used.